REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

After entry of the foregoing amendment, Claims 1-11 are pending in the present application. Claims 1-9 are amended and Claims 10 and 11 are added by the present amendment without introduction of any new matter.

In the outstanding Office Action, the specification was objected to; the title was objected to; the drawings were objected to; Claims 1-9 were rejected under 35 U.S.C. 112, second paragraph; and Claims 1-9 were rejected under 35 U.S.C. 102(b) as anticipated by Kunikiyo (U.S. Patent No. 5,845,105).

Regarding the objections to the specification, the specification is amended in view of the Examiner's comments. Accordingly, Applicants respectfully request that the objections to the specification be withdrawn.

Regarding the objections to the drawings, Figures 7-11 are amended to include the legend "Background Art." Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

Regarding the rejection of Claims 1-9 under 35 U.S.C. 112, second paragraph, those claims are amended in view of the Examiner's comments.[1] With respect to the recitation of the "normal equation," Applicants note that the term "normal equation" is known in the art (e.g., see Attachment I). Accordingly, Applicants respectfully request that the rejection be withdrawn.

Turning now the rejection of Claims 1-9 under 35 U.S.C. 102(b), as anticipated by Kunikiyo, that rejection is respectfully traversed.

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[1] For support, see Specification, page 13, line 3 – page 20, line 16.

Amended Claim 1 is directed to a method of simulating variations in first and second electrical characteristics of a semiconductor integrated circuit. The method includes:

> (a) forming a corner model including at least one corner defining predetermined limits of said variations of said first and second electrical characteristics;
>
> (b) assigning said variations in said first and second electrical characteristics at said at least one corner as respective predetermined values;
>
> (c) performing a circuit simulation to determine respective device parameter sensitivities of said first and second electrical characteristics at said at least one corner, the device parameter sensitivities representing respective derivatives of said first and second electrical characteristics with respect to a device parameter; and
>
> (d) applying said device parameter sensitivities and said predetermined values to a normal equation of the least squares method, and solving the normal equation to determine variations in said device parameter at said at least one corner.

Amended independent Claim 8 recites a device performing similar operations. Claims 1-7 and 9 depend directly or indirectly from independent Claims 1 and 8.

By way of background, Figure 9 illustrates a corner model reflecting electrical characteristics for a CMOS device having NMOS and PMOS transistors. Point P0a reflects the typical saturation current values for the NMOS and PMOS transistors Idsatn and Idsatp, which correspond to device parameter values L, W, Tox, and Vth0.[2] The four corners P1a-P4a reflect limits for variations in the typical NMOS and PMOS saturation current values δIdsatn and δIdsatp, which correspond to variations in the device parameter values $\delta(\Delta L)$, $\delta(\Delta W)$, δTox, and δVth0.[3]

Figure 11 illustrates a conventional method of determining a device parameter set at each corner of a corner model.[4] As shown, the method can require repeated circuit simulations and re-adjustments of the device parameter set, i.e., trial and error.[5] Conversely,

[2] Specification, page 2, lines 18-21.
[3] Specification, page 2, lines 21-24.
[4] Specification, page 6, lines 3-8.
[5] Specification, page 8, lines 8-16.

the present invention determines a unique device parameter set at each corner without repeated circuit simulations and re-adjustments.[6]

In a non-limiting example, Figure 1 illustrates an embodiment of the present invention. In steps S02 and S03, the parameter sensitivities of each electrical characteristic, as defined at the corners of the corner model, are determined via circuit simulation.[7] In step S04, the corresponding variations in each device parameter $\delta(\Delta L)$, $\delta(\Delta W)$, δTox, and $\delta Vth0$ are then calculated from a normal equation of the least squares method.[8]

The outstanding Office Action cites Figure 10 of Kunikiyo as teaching the claimed corner model. However, Figure 10 is not taught as a corner model. Rather, Figure 10 is only taught as a "graph showing electrical characteristics of a transistor by changing a process condition."[9] Moreover, the "corners" do not define predetermined limits of variations in electrical characteristics. Rather, the "corners" merely correspond to measured values for particular wafers.[10] Accordingly, the graph is only disclosed for determining "optimum" process conditions,[11] and not for determining variations in such process conditions. In fact, all of Kunkiyo's teachings are directed to determining optimum process parameters.[12]

The Office Action asserts that Figure 10 enables a method for arbitrarily choosing at least one corner defining a limit of variations in electrical characteristics. However, Applicants respectfully note that, assuming arguendo, Kunikiyo's Figure 10 is enabling, it would only be enabling based on a hindsight application of the teachings of Applicants' invention, whereby the noted Figure 10 conceivably could be interpreted to derive Applicants' invention. Of course, the teachings of Applicants' invention cannot be applied in an analysis under 102(b). Therefore, as the choosing of at least one corner from Figure 10 to

[6] Specification, page 12, lines 2-5.
[7] Specification, page 19, line 22 – page 20, line 2.
[8] Specification, page 20, lines 3-6.
[9] Kunikiyo, col. 5, lines 66-67.
[10] Kunikiyo, col. 3, lines 3-6.
[11] Kunikiyo, col. 3, lines 12-16.
[12] Kunikiyo, Abstract, col. 7, lines 17-23.

define a limit of variations in electrical characteristics is not evident from the reference, the rejection of Claims 1-9 under 35 U.S.C. 102(b) as anticipated by Kunikiyo is respectfully traversed. If the Office Action is asserting that the teachings of Kunikiyo could be modified to anticipate the features of the claimed invention, then a § 103 rejection citing motivation in the prior art reference itself, not Applicants' disclosure, for such a modification is required.

The Office Action cites step 50 of Figure 13 and Equation 3 of Kunikiyo as teaching the claimed device parameter sensitivities. The claimed device parameter sensitivities represent ***respective*** derivatives of the first and second electrical characteristics, with respect to a device parameter. On the other hand, Equation 13 of Kunikiyo represents a derivative of a sum of squares formula S incorporating all electrical characteristics. As Equation 13 does not treat each electrical characteristic separately (i.e., respectively) with respect to a device parameter, Equation 13 does not teach the claimed device parameter sensitivities.

In addition to the above distinctions, Applicants note that the claimed invention further distinguishes over Kunikiyo in the following respects. First, the claimed invention determines a parameter set at a corner of a corner model, while Kunikiyo determines a parameter set represented in the form of a response surface, as shown in the formulas (1), (7), and (10) of Kunikiyo. Second, the claimed invention determines a parameter set from a normal equation based on a circuit simulation. Kunikiyo determines a parameter set from a multinomial equation based on a characteristic of a response surface. Third, the claimed invention utilizes device parameter sensitivities that allow a linear assumption of a variation of those sensitivities. Kunikiyo teaches only the determination of an optimum value.

Accordingly, for the reasons stated above, Applicants respectfully request that the rejection of Claims 1-9 under 35 U.S.C. 102(b), as anticipated by Kunikiyo, be withdrawn.

Applicants note that Claims 8 and 9 are amended and new Claims 10 and 11 are added to recite the claimed invention in a different statutory scope. More particularly, Claims

8 and 9 are amended to recite each of their claimed features in non-means-plus-function terminology. Claims 10 and 11 are added to correspond to amended Claims 8 and 9, respectively, but recite the data processing unit of amended Claim 8 in means-plus-function terminology. Support for the amendments to Claims 8 and 9 and the addition of Claim 11 is self-evident from the claims as originally filed. Support for the recitation of the "data processing means" of Claim 10 may be found in at least the fourth embodiment disclosed by the Specification at page 26, line 16 – page 29, line 22.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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ATTACHMENT I

Normal Equation

Given an overdetermined matrix equation

$$\mathbf{A}\mathbf{x} = \mathbf{b},$$

the normal equation is that which minimizes the sum of the square differences between left and right sides

$$\mathbf{A}^{\mathrm{T}}\mathbf{A}\mathbf{x} = \mathbf{A}^{\mathrm{T}}\mathbf{b}.$$

SEE ALSO: Least Squares Fitting, Moore-Penrose Matrix Inverse, Nonlinear Least Squares Fitting, Pseudoinverse

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